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(54) Low voltage, switched capacitance circuit employing switched operational amplifiers with maximized voltage swing

(57) A switched capacitance circuit functioning with unboosted control phases and using at least as an input switch of said switched capacitance a switched operational amplifier structure is provided with a switch for switching the output of the input operational amplifier to the supply node during an OFF-phase of the operational amplifier and another switch for switching to ground the output node of the switched capacitance during an ON-phase of said input operational amplifier in order to prevent charge losses via the substrate of the turn-on switches of the circuit. Precision is retained while ensuring a rail-to-rail dynamic range. Special arrangements may be implemented for controlling the amplitude of switching spikes when so required. A fully differential embodiment is also feasible with additional advantages.

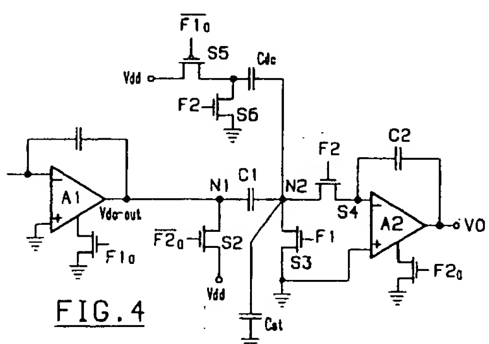

FIG.4

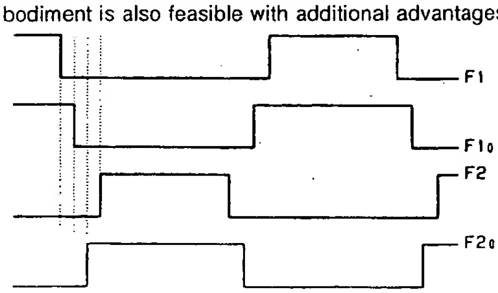

FIG.5

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The present invention relates to switched capacitance (SC) circuits particularly for low supply voltage and low power absorption employing at least as an input switch a so-called switched operational amplifier structure in order to ensure a high conductivity of the input switch under any signal condition.

Switched capacitance circuits are widely used for signal processing because of their extremely low distortion figure and because they are easily integrated. Filters of any kind are commonly implemented by switched capacitance circuits.

In low supply voltage and low current absorption applications, typically in battery powered circuits, it is often required that the circuits may be powered with relatively low supply voltages, down to a level of about 1.5V. In these conditions, ensuring an effective driving of the switches that are commonly constituted by field effect transistors (FET) and more commonly MOSFET becomes problematic. In fact, if the supply voltage drops to levels that are comparable with those of the threshold voltage of field effect transistors, the correct functioning of classical switched capacitance circuits, as the integrator depicted in Figure 1, is quickly jeopardized. In fact, in order to ensure a correct functioning of the input switch S1, the overdrive voltage of which depends on the input signal, the dynamic range of operation of the circuit is drastically reduced.

A solution to the problem that has been proposed for ensuring to the switches and in particular to the input switch S1, a high conductance under any condition of the input signal is based either on the use of special fabrication technologies for realizing the switches with low threshold transistors or by using special circuits (voltage multipliers) for multiplying the clock voltage with which the switches may then be suitably overdriven. This second approach, though avoiding complication of the fabrication process for implementing low threshold integrated devices, requires on the other hand the integration of dedicated voltage multipliers.

Lately an alternative solution based on the use of a switching structure defined "Switched-Opamp", that is based on the use of a switched operational amplifier has been presented in the article: "Switched-Opamp, a Technique for Realising Full CMOS Switched-Capacitor Filters at Very Low Voltages" by M. Steyaert, J. Crols and S. Gogaert, IEEE Proc.

According to this new approach, in order to ensure to the switches and in particular to the input switch S1 a high conductivity under any signal situation, the MOSFET structure, typically a CMOS gate, that was conventionally used as the input switch S1 is substituted with a switched operational amplifier which is driven to turn on and off by a dedicated switch. The other switches that compose the switched capacitance structure may be realized with transistors of the same type, for example with N-channel or with P-channel transistors, without necessarily requiring the use of CMOS structures.

For illustrating this technique, Figure 2 shows a classical switched capacitance integrator functionally equivalent to the circuit depicted in Figure 1, wherein the function of the input transistor S1 is performed by the switched operational amplifier A1.

Although the use of a switched operational amplifier as an input switch of a switched capacitance circuit offers decisive advantages as compared with the circuits of the prior art, it is unable of maximizing the dynamic characteristics of the circuit under any working condition, compatibly with the necessity of ensuring the turn-off of the switches under any conditions. By referring to the circuit of Figure 2, if the voltage Vref is made equal to Vdc_out, the maximum voltage swing that can be obtained, while ensuring the turning off of the switches, will be equal to 2 (Vref-Vdsat).

On the other hand, in order to ensure a high conductivity of the input switch, Vref must be placed at the lowest possible level for an N-channel switch or to the highest possible level for a P-channel switch. In this way though, the dynamics of the operational amplifiers (A1 and A2) employed in the circuit is markedly reduced.

In other words, the value Vdc_out is tied to the Vref value, thus imposing a compromise choice that is strictly tied to the contemplated operating conditions of the switched capacitance circuit.

The quest for a switched capacitance circuit suitable for low supply voltage and low current absorption applications which would not require boosted timing signals while ensuring under any conditions of the input signal a dynamic behaviour that is practically equal to the maximum voltage swing, that is rail-to-rail dynamics, has lately brought the authors of the present invention to develop a circuit described in the article: "Design strategy for low-voltage SC circuits", published in "Electronic Letters", 3rd March 1994, Vol. 3, Nr. 5, the content of which is herein incorporated by express reference.

Basically, the solution proposed in that article, employs as an input structure a switched operational amplifier, whose input common mode voltage is made null in order to ensure both a correct operation of the switches and the maximum dynamic range possible. Such a null value of the input common mode voltage is imposed by a bias capacitor that regulates, through a mechanism of charge injection, the virtual ground voltage, by "advance knowledge" of the output common mode voltage of the same input switched operational am-

plifier.

As shown in the scheme of Figure 3 which represents an embodiment of the circuit described in the above noted article, a nullifying of the input common mode voltage is achieved by means of the additional capacitor Cdc suitable to inject electrical charge on the output node N2 of the switched capacitance C1 at every switching; the capacitor Cdc being switched by the pair of switches S5 and S6, alternatively to the supply voltage Vdd and to ground. The circuit is controlled by a pair of clock phases: 1 and 2.

Despite the fact that the circuit of Figure 3, described in the above noted article, is capable of ensuring a maximum dynamic range also with relatively low supply voltages without requiring the generation of boosted driving clock phases, it presents several drawbacks.

At a certain switching instant (during an integration phase), the capacitance C1 and C2 charge to a certain voltage, and more precisely to the voltage of the output node of the input operational amplifier A1, the capacitor C1 and to the voltage of the output node of the circuit, that is of the operational amplifier A2, the feedback (integrating) capacitor C2 of the operational amplifier A2 of the output structure of the circuit.

Immediately after said switching instant, the positively charged armatures of the capacitors C1 and C2 are connected to ground and therefore the other armatures of the capacitors (that is the node N1 at the start of the clock phase 1 and the node N2 at the start of the clock phase 2) are forced to assume a negative voltage (below ground).

In particular, the node N2, at the start of the control phase 2, and the output node N1 of the input operational amplifier A1, at the start of the phase 1, are forced to assume a negative voltage (below ground).

If the switches S4 and S2 are made with an N-channel field effect transistor integrated in a grounded substrate, the biasing at a negative voltage (below ground) of a current terminal of an integrated N-channel switch (transistor) causes a direct biasing of the junction between the source or drain node of the transistor and the substrate, thus determining a loss of charge (and therefore of signal) via the substrate itself.

Even if such an effect occurs only during transitions from a state to the other, the loss of signal may be sufficient to degrade the otherwise intrinsic precision of a switched capacitance circuit (SC) and this may be untolerable in many applications.

On the other hand, a simple solution of the above noted problem of signal degradation could he that of dimensioning the Cdc capacitance in such a way as to bias the inputs of the operational amplifiers A1 and A2, respectively of the input and the output structures of the switched capacitance circuit, at a higher than zero (ground) level, but in this way again the dynamic range would be reduced.

A main objective of the present invention is to provide an improved switched capacitance circuit, free of the above noted drawbacks and/or limitations of the known circuits.

According to a first aspect of the present invention, the output of an input switched operational amplifier structure of the switched capacitance circuit is switched to the supply voltage Vdd, instead of to ground as in the circuit described in the above noted article. This is implemented by employing a dedicated integrated P-channel switch in a substrate that is connected to the supply voltage Vdd and therefore exempt of the so-called "body effect". In this way, the output node of the input operational amplifier A1 will not assume a negative voltage during the phase of operation when the switched operational amplifier is off. Moreover, the clock phases that drive the two switches that connect the bias capacitor Cdc, respectively to the supply node and to ground, are exchanged in order to subtract instead of summing a Vdd/2 voltage.

As a consequence, both the switched capacitance C1 and eventually also the feedback capacitance of an integrating output stage (second operational amplifier) functions in a way that, during switchings, the potentials of the output node of the input operational amplifier and of the output node of the switched capacitance C1 rise, thus preventing any loss of charge via the respective substrates of the integrated switches.

The capacitance Cdc, in controlling the input common mode, brings the virtual ground node to a negative value during switchings, in other words, substantially generates negative spikes.

According to a further aspect of the present invention, when these negative spikes may interfere and/or be prejudicial to the correct operation of the integrated circuits as a whole, the amplitude of these spikes may be markedly reduced by adding a capacitance between the output node of the switched capacitance and ground, in order to distribute over a larger capacitance the charge injected on said node by the Cdc capacitor at the switching instants.

According to a further aspect of the present invention, the amplitude of these negative spikes may be strongly depressed by anticipating the turning on of the switched operational amplifiers and thus delaying the connection of the switched capacitance C1 to the virtual ground node. This may be easily obtained by driving the relative switches with suitably delayed (or anticipated) clock phase signals. In fact the contribution of these anticipated connections tend to rise the po-

tential on the output node of the switched capacitance during switchings. In this way, the connection of the biasing capacitor Cdc and therefore the consequent injection of charge on the output node of the switched capacitance is delayed thus regulating the input common mode while producing negative spikes of relatively reduced amplitude.

The different aspects and advantages of the circuit of the invention will become even more evident through the following description of several important embodiments and by referring to the annexed drawings, wherein:

Figure 1 shows a classic scheme of a SC integrator employing CMOS switches according to the prior art;

Figure 2 shows a switched capacitance circuit functionally similar to the circuit of Figure 1, wherein the function of the input switch is performed by a switched operational amplifier structure, according to a known technique;

Figure 3 shows a circuit functionally similar to the circuit of the preceding figures suitable to permit a maximum dynamic range, according to a more recently developed technique;

Figure 4 is a basic diagram of a circuit made in accordance with the present invention;

Figure 5 is a diagram of the control clock phases of the circuit of Figure 4, according to an embodiment of the invention;

Figure 6 is a basic diagram showing the circuit of the invention realized in a fully differential form.

A switched capacitance integrator made according to a preferred embodiment of the present invention is depicted in Figure 4. As may be noticed, the switch S2 connects the node N1 to the supply voltage Vdd instead of to ground as in the known circuit of Figure 3. Moreover, the driving clock phases of the switches S5 and S6 that connects to Vdd or to ground the bias capacitor Cdc are exchanged, in order to functionally subtract a voltage equal to Vdd/2 instead of summing it as in the known circuit of Figure 3.

As a consequence, the output node N1 of the input operational amplifier A1, during a phase in which the switched operational amplifier is off, will not assume a negative (below ground) voltage but a voltage given by Vdd-Vo. In this way, the feedback capacitor C2 of the output integrating stage (that is of the second switched operational amplifier A2) wil not lose any charge.

Therefore, the sampling capacitance C1 as well as the feedback capacitance C2 of the output integrating stage function in a way that, during switchings, the potentials of the nodes N1 and N2 rise so as to prevent a loss of charge via the respective substrates of the switches S2, S3 and S4.

On the other hand, in fixing the input common mode, the capacitor Cdc forces the virtual ground of the operational amplifier A2 to a negative voltage (below ground) at the switching instants, thus producing negative voltage spikes. Whenever this cannot be tolerated, the amplitude of the generated spikes may be markedly reduced through the sole or combined action of other circuital arrangements of the present invention.

According to a first of these other aspects of the invention, the amplitude of the switching spikes produced by the injection of charge effected by the capaciter Cdc on the node N2 may be strongly depressed by adding a capacitor Cst, connected between the node N2 and ground, as shown in Figure 4.

In this way the charge injected by the biasing capacitor Cdc is distributed over an augmented capacitance and therefore the node N2, at the switching instant, assumes a negative (below ground) potential but of a much reduced amplitude as compared with the one that would result without the introduction of the buffer capacitance Cst.

A further aspect of the circuit of the invention suitable to reduce the amplitude of the negative switching spikes consists in anticipating the turning on of the input switched operational amplifier A1 and of the output switched operational amplifier A2, as referred to the instant of connection to the virtual ground of the switched capacitance C1 through the switches S6, S4 and S3.

Of course this may be easily implemented by driving the switches with clock phase signals suitably delayed in respect to the homologous clock phase signals that turn on the operational amplifiers A1 and A2 and drive the switches S5 and S2.

The direct phases of the driving clock signals, according to such a preferred embodiment of the invention, are depicted in Figure 5.

In the shown example, the switch S2 toward the supply voltage Vdd is realized with a P-channel field effect transistor having a substrate connected to the supply voltage Vdd, therefore the transistor is not affected by the so-called "body effect".

The improved SC circuit of the invention, while functioning without requiring boosted control phases and with a maximum dynamic range (rail-to-rail) as normally contemplated in low supply voltage applications and with a reduced current absorption, retains the precision of the circuit within the limits imposed to a SC structure, by eliminating any charge loss via the substate of turned on switches.

The switched capacitance circuit of the invention provides an output signal only during a clock phase.

In designing filters of a high order, it is often necessary to implement sign inversions by adding

a further stage. Another aspect to be considered in these cases is the increase of the offset caused by the possible error that may be made in a switching phase by the charge injection Cdc. Both these limitations can be eliminated by adopting a fully differential circuit topology, as depicted in Figure 6.

By choosing Vref=0, Vdc_in=0 and Vdc_out=Vdd/2, the dynamic range doubles as compared with the case of a single-ended circuit of Figure 4. Moreover, by virtue of the fully differential topology of the circuit, it is intrinsically available the option to invert the sign of the output signal by simply crossing over the signal lines. Finally, all the errors that may be caused by the switchings of the switches (especially of the switches that connect the bias capacitor Cdc) may be considered as common mode and will not influence the precision of the differential output signal.

Claims

1. A switched capacitance circuit functioning with unboosted clock phases employing a switched operational amplifier (A1) as an input switch of a switched capacitance (C1) and having means for freeing the definable level of the output DC voltage (Vdc-out) of said switched operational amplifier (A1) from a predefined value of a reference voltage of discharge of the switched capacitance (C1) and to fix said level of the output DC voltage (Vdc_out) of said operational amplifier (A1) to a value corresponding to about half the supply voltage (Vdd), said means comprising a bias capacitor (Cdc) having an armature connected to the output of said switched capacitance (C1) and the other armature that is connectable through a first switch (S5) to the supply node (Vdd) and through a second switch (S6) to ground,
   characterized by comprising
   a third switch (S2) switching the output (Vdc_out) of said switched operational amplifier (A1) to the supply voltage (Vdd) during a turn-off phase of said operational amplifier (A1);
   a fourth switch (S3) switching said output node of the switched capacitance (C1) to ground during a turn-on phase of said operational amplifier (A1).

2. A circuit as defined in claim 1, characterized by further comprising a buffer capacitor (Cst) connected between said output node of the switched capacitance (C1) and ground.

3. A circuit as defined in claim 1, characterized by comprising an output switch structure composed of a second switched operational amplifier (A2) having a non inverting input connected to ground and an inverting input functionally connected to said output node of the switched capacitance (C1) through a fifth switch (S4).

4. A circuit according to claim 3, wherein said fourth switch (S3) is closed and opened with a certain lead time in respect to the closing and opening of said first switch (S5) and of a switch for turning on and off said input operational amplifier (A1) and wherein said second switch (S6) and said fifth switch (S4) are closed and opened in phase with each other with a certain lead time in respect to the closing and opening of said third switch (S2) and of a switch for turning on and off said second switched operational amplifier (A2).

5. A circuit as defined in claim 3, wherein each of said first switch (S5) and said third switch (S2) is realized with a P-channel field effect transistor and each of said second (S6) fourth (S3) and fifth (S4) switches is realized with an N-channel field effect transistor.

6. A circuit as defined in claim 1, characterized by being realized in a fully differential form, by duplicating said means and said switches for each of the two differential outputs of the input switched operational amplifiers, each driving a switched capacitance.

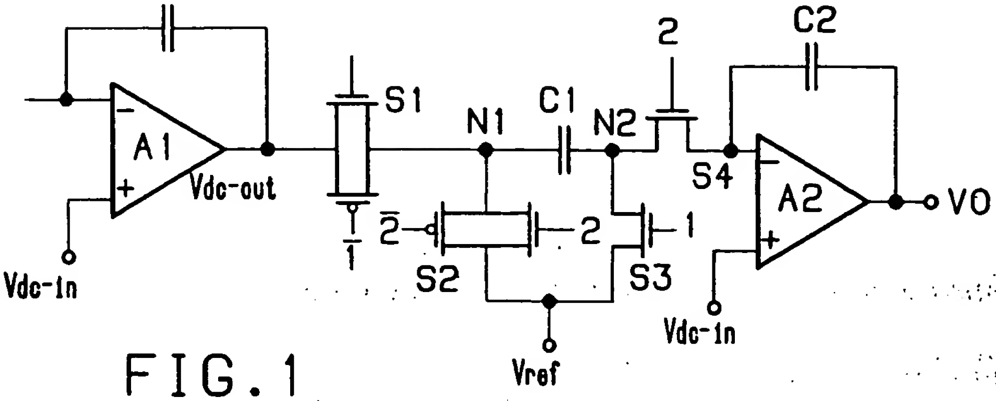


FIG.1

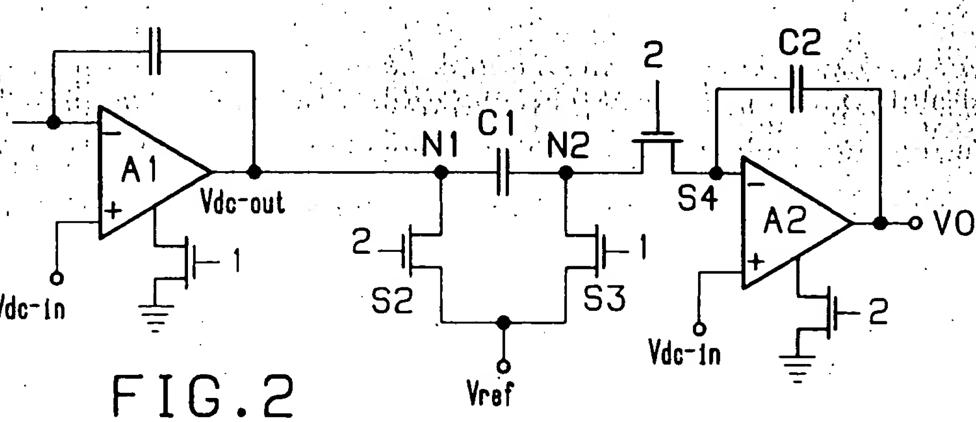


FIG.2

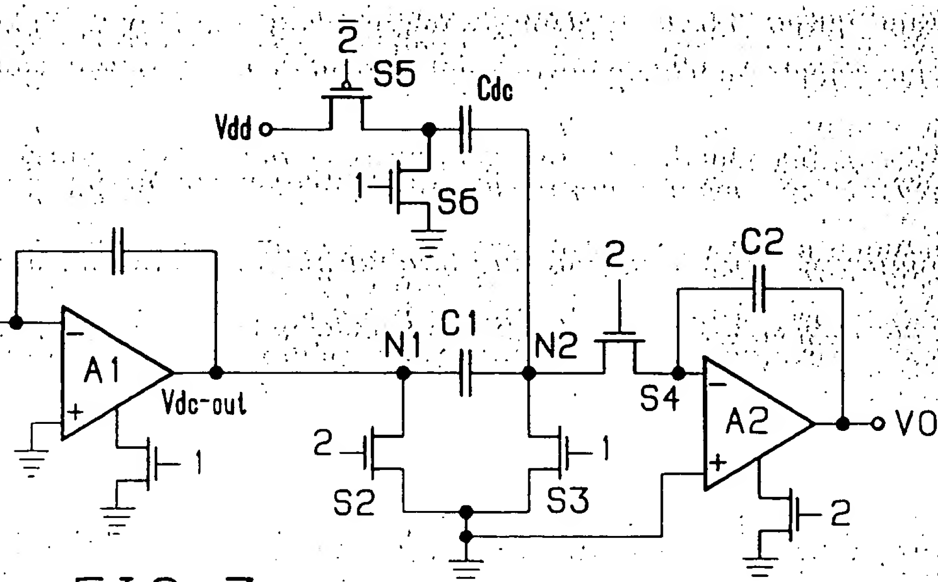


FIG.3

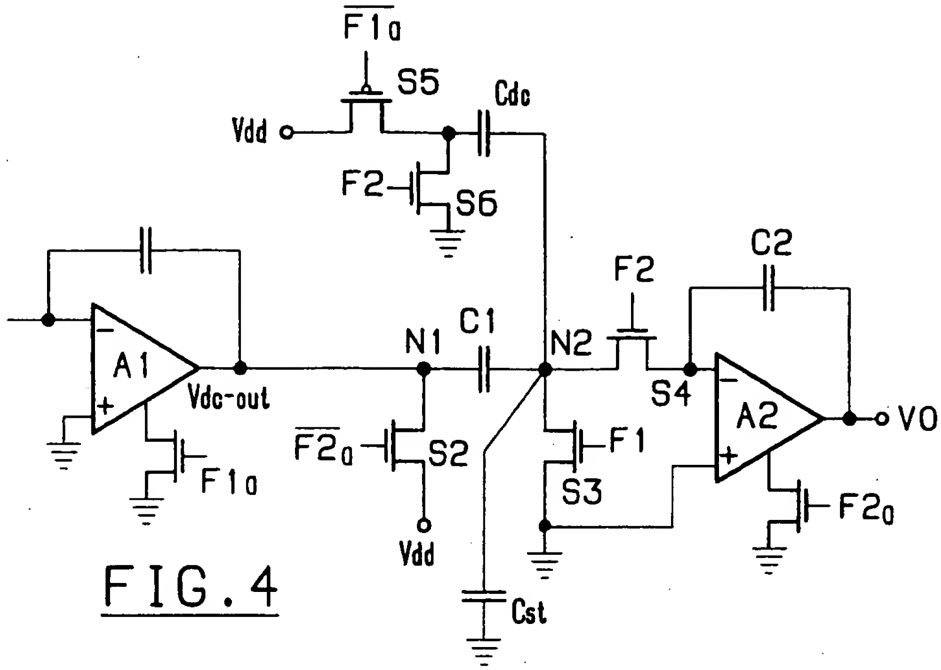

$\overline{F1a}$
S5
Cdc
Vdd
F2
S6
C2
F2
N1
C1
N2
A1
Vdc-out
S4
A2
VO
$\overline{F2_0}$
S2
F1
F1a
S3
$F2_0$
Vdd
Cst

FIG.4

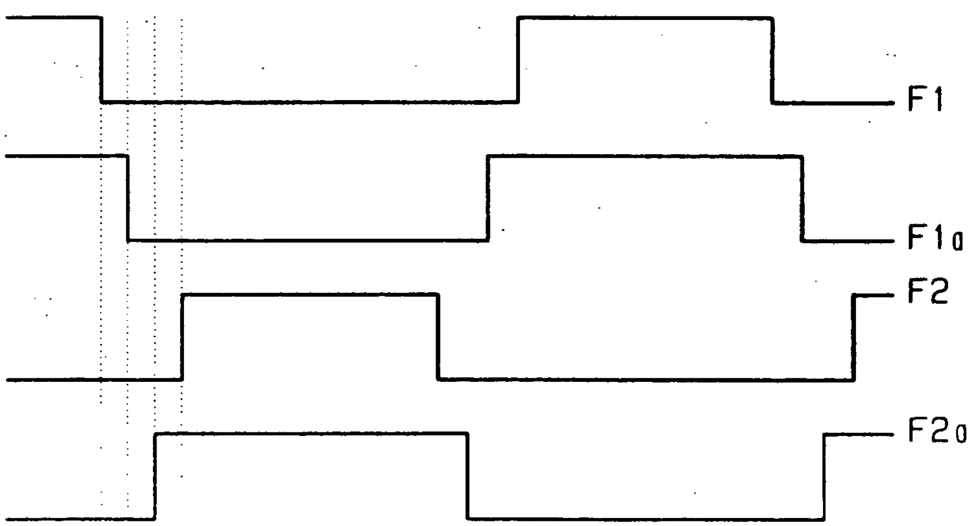
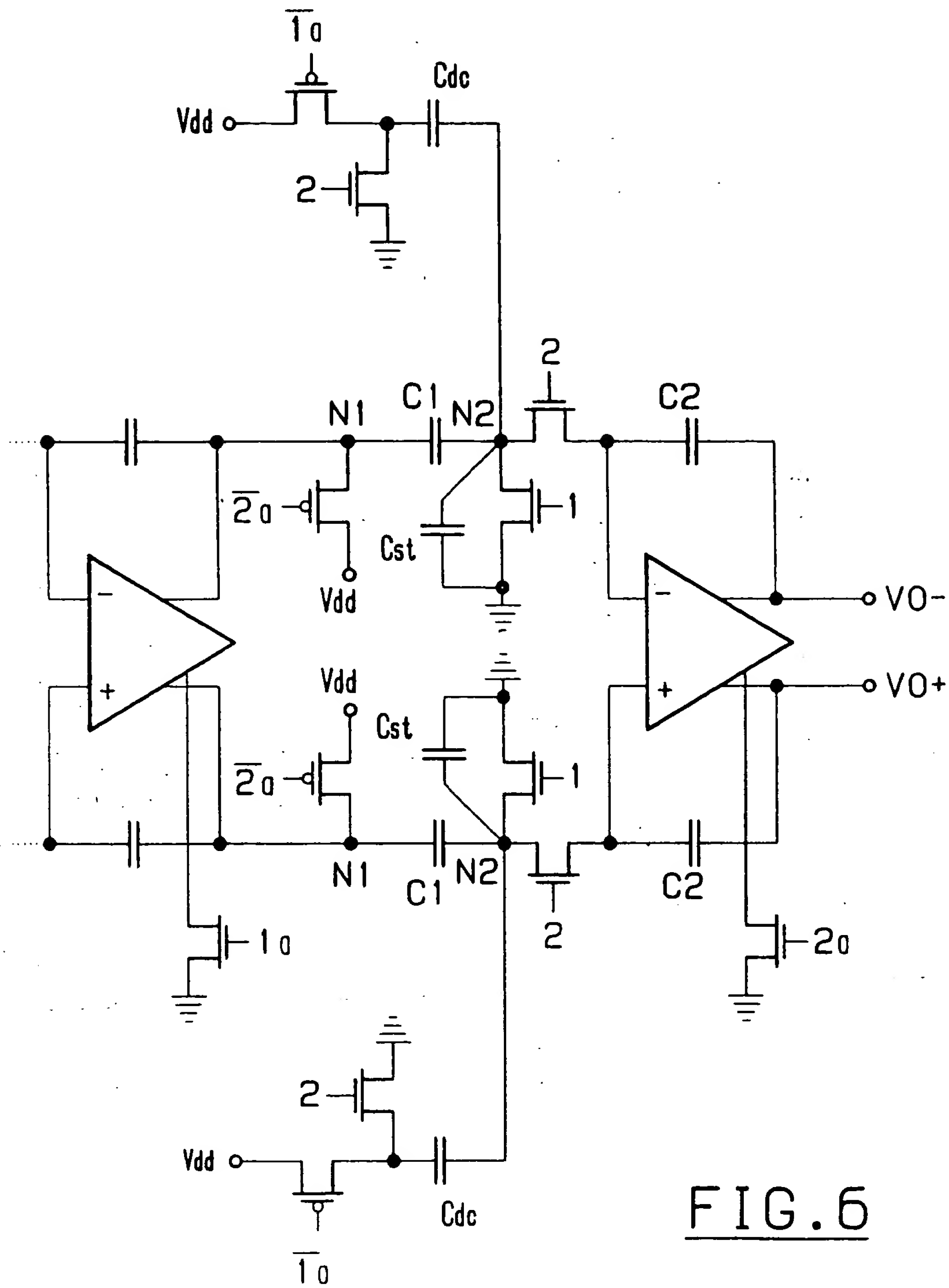

F1
F1a
F2
$F2_0$

FIG.5



1a
Vdd
Cdc
2
N1
C1
N2
2
C2
2a
1
Cst
Vdd
VO-
VO+
Vdd
Cst
2a
1
N1
C1
N2
C2
2
1a
2a
2
Vdd
Cdc
1a

FIG.6

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EUROPEAN SEARCH REPORT

Application Number
EP 94 83 0318

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
D,A	ELECTRONICS LETTERS., vol.30, no.5, 3 March 1994, ENAGE GB pages 378 - 380, XP442897 A. BASCHIROTTO ET AL 'DESIGN STRATEGY FOR LOW-VOLTAGE SC CIRCUITS' * the whole document * -----	1-6	H03H19/00
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H03H H03F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	24 November 1994	Coppieters, C

CATEGORY OF CITED DOCUMENTS

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